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Modified SPWM technique for single phase variable voltage nine level inverter for PV system

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ABSTRACT

Multilevel inverters are widely popular because they boost the overall staging of the network with low harmonic distortion, less strain, and simply create highest possible development in industrial and electrical vehicle applications. Here a hybrid multilevel inverter having few switches compare to traditional multi-level inverters has been implemented. It has the capability to operate as a 3-level, 5-level, 7-level and 9-level inverter with different magnitudes of output voltage by varying the modulation index without changing of circuit topology and switching sequences. A new variable amplitude phase opposition disposition sinusoidal pulse width modulation (VAPODPWM) technique is proposed to control the inverter. In this concept unsymmetrical carrier wave form, i.e. A single triangular wave is divided into three triangular waves of different magnitude was chosen. it reduces the volt-sec of output due to that it gives less total harmonic distortion (THD) compare to other conventional space pulse width modulation (SPWM) techniques and conventional space vector pulse width modulation (CSVPWM) control techniques. The ease of conversion capability with less count of switches and operation with less THD shows the effectiveness of the converter. The converter is simulated by using MATLAB/Simulink and results are discussed.

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1. INTRODUCTION

Most modern PV, wind, industrial and electric vehicle systems can be operated with multilevel inverters due to the advantages of multilevel inverters, such as reduced total harmonic distortion (THD), reduced switch count, reduced switch voltage stress, reduced losses, and increased efficiency. Compared to conventional converters, which needed two stages of conversion for PV system applications, it offers single step conversion. In order to maintain uninterrupted operation in PV system applications in the presence of fault circumstances, the power converter's reliability is required.

Numerous researchers have created various multilevel inverters because to the straightforward functioning and reduced THD of multilayer inverters. The development of different multilayer inverters, such as diode clamped, cascaded, and flying capacitor inverters, and the implementation of their control may be found in [1]. In order to achieve a pure sine wave, the number of levels must be increased, which necessitates an increase in the number of switching devices. However, this increases circuit complexity therefore

complexity can be decreased by reducing the number of switching devices with better THD values are accomplished in [2]–[6]. Many sinusoidal pulse width modulation PWM approaches, third harmonics injection sinusoidal PWM method, and space vector pulse width modulation methods are utilized by various researchers [7], since the quality of the output voltage of MLI is determined by the value of THD. According to [8], in [9], the MLI will lower the harmonics, lowering the price of filters. Continuity of supply is very important during the fault of open circuit or short circuit of switches hence the concept of fault tolerant operation was analyzed in references [10]–[12]. The output was yielded with varying DC levels based on the correct ON and OFF switching sequence of the devices to achieve the AC voltage, and the fundamental component of the output voltage rose by reducing the higher order harmonics [13]. Several PWM approaches are examined, including the fixed carrier frequency and variable carrier frequency concepts, to reduce harmonics in [14] although it obtains the higher THD nearly 20%. Many researchers are looking into various innovative swathing approaches to get rid of harmonics and enhance the output wave shapes shown in [15]. A novel 7-level MLI that has more switches and produces good results with lower THD has been created [16]. The topology of a new seven-level inverter, which has more components and a worse THD, was proposed in [17]. The advanced nine level inverters are introduced with less no of devices but THD was not better one represented in [18]–[20]. A modified SPWM technique was used in [21] to reduce THD; the carrier signal was split into three equal parts and the signal was changed, although the THD was higher than with the suggested technique. By increasing levels and adjusting the conduction time of the gating signal, the THD of the cascaded H-bridge multilevel output voltage can be decreased to a lower value, as detailed in [22], [23].

A revolutionary MLI with fewer switching devices was described in [24] order to obtain more level with lower THD. In order to lower THD of MLI, a unipolar carrier technique was presented in [25]. It is possible to lower the THD of the inverter's output voltage by adding more levels, but doing so makes the system more complex and costs more money. Therefore, it is necessary to obtain pure sinusoidal wave form without adding more levels by lowering the THD of the voltage with fewer components and fewer levels. So, a new, advanced topology with fewer components is suggested here to lower the THD of voltage. Additionally, a number of pulse width modulation techniques are used to produce pure sine waves.

2. CIRCUIT CONFIGURATIONS

2.1. 5-Level operation

This hybrid 5-level multilevel inverter fit by 3-level diode clamped inverter and half bridge inverter which is displayed in Figure 1 [10]. Here a pair of DC sources with equal-sized i.e., $E_{dc}/2$ is applied to the above inverter and also R-L load is connected between a 3-L diode clamped inverter and a half bridge inverter. Under standard conditions, the inverter's output voltage is composed of five levels: $+E_{dc}$, $+E_{dc}/2$, 0, $-E_{dc}/2$, and $-E_{dc}$, which are attained via the appropriate switching order shown in Table 1. This inverter also has the capability to operate as a fault tolerant during fault of switches, which is referred in [10]–[12].

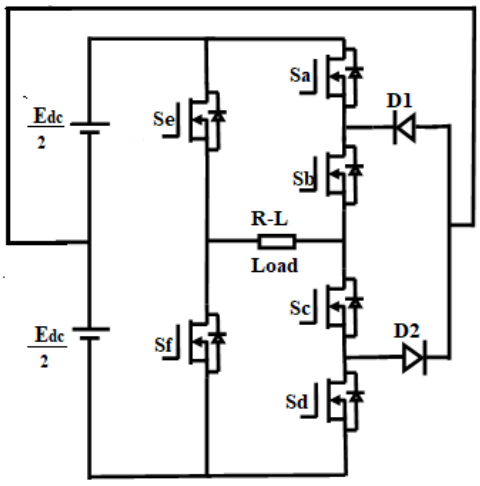

Figure 1. 5-Level inverter

Table 1. Switching pattern for 5-level mode

Voltage Level	Activate switches
+ E_{dc}	S_a, S_b, S_f
+E_{dc}/2	S_b, S_c, S_f
0	S_c, S_d, S_f
	S_a, S_b, S_e
-E_{dc}/2	S_b, S_c, S_e
- E_{dc}	S_c, S_d, S_e

2.2. 7-Level operation

By adding one bidirectional switch and make of unsymmetrical sources of above one, this topology can also function as a seven-level inverter. However, under normal operating conditions, there is no need to use the bidirectional switch S_g, it can also function as a surplus switch in the case of zero level and fault conditions in the five-level inverter. The sources of unsymmetrical such that upper source regarded as (2/3) E_{dc} and lower source as (1/3) E_{dc}, which is shown in Figure 2. The peak of output voltage of 7-L inverter has same as a 5-level inverter and has seven levels: +E_{dc}, +(2/3) E_{dc}, +(1/3) E_{dc} 0, -(1/3) E_{dc}, -(2/3) E_{dc}, and -E_{dc}. The converter switching pattern for the 7-level operation is demonstrated in Table 2.

2.3. 9-Level operation

The operation of above 7-level inverter was extended to 9-Level inverter i.e Figure 3 by ad of two more sources such that four sources of equal magnitudes i.e E_{dc}/4 are applied to the above 5-level inverter. Increasing of levels cause the output voltage of the inverter is pure sinusoidal with less THD. The output voltage of inverter of 9-L, i.e., +E_{dc}, +3/4 E_{dc}, +1/2 E_{dc}, +1/4 E_{dc}, 0, - E_{dc}/4, - E_{dc}/2, -3/4 E_{dc} and -$E_{d,}$ are obtained by switching the switches according to Table 3. This topology has less no of components compare to the other conventional multilevel inverters are shown in Table 4.

Table 2. Switching pattern for 7-level mode

Voltage Level	Activate switches
+ E_{dc}	S_a, S_b, S_f
+(2/3)E_{dc}	S_a, S_b, S_g
+(1/3)E_{dc}	S_b, S_c, S_f
0	S_b, S_c, S_g
-(1/3)E_{dc}	S_c, S_d, S_g
-(2/3)E_{dc}	S_b, S_c, S_e
-E_{dc}	S_c, S_d, S_e

Table 3. Switching pattern for 9-level mode

Voltage Level	Activate switches
+ E_{dc}	S_a, S_b, S_f
+(3/4)E_{dc}	S_b, $S_{f,}$ D_1
+(1/2)E_{dc}	S_a, $S_{b,}S_g$
+(1/4)E_{dc}	$S_{b,}S_{g,}$ D_1
0	S_a, $S_{b,}$ S_e
-(1/4)E_{dc}	S_c, $S_{g,}D_2$
-(1/2)E_{dc}	S_c, $S_{d,}$ S_g
-(3/4)E_{dc}	S_c, $S_{e,}$ D_2
-E_{dc}	S_c, S_d, S_e

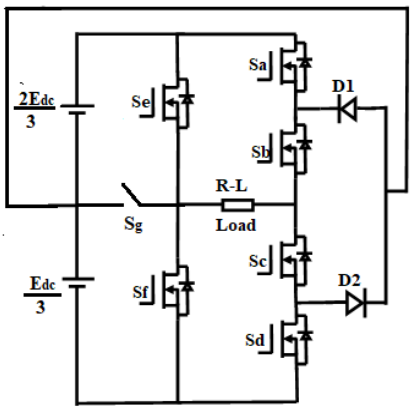

Figure 2. 7-Level inverter

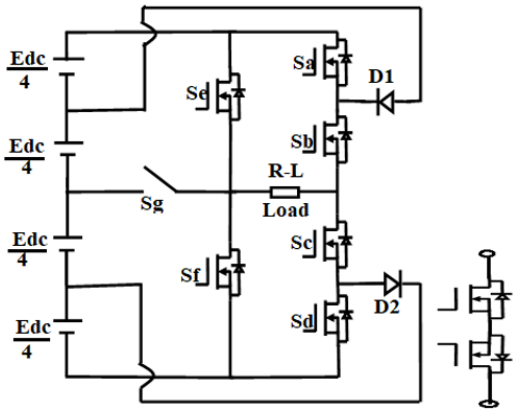

Figure 3. 9-Level inverter switch (S_g)

Table 4. Components comparison of 9-level inverter with other MLI

Components/peTy	NPC	Flying Capacitor MLI	Cascaded MLI	Hybrid 9-Level MLI
No of DC Sources	8	8	4	4
No of flying capacitors	0	28	0	0
DC bus capacitors	8	8	4	4
No of clamping diodes	56	0	0	2
No of main switches	16	16	16	7

3. MODULATION CONTROL SCHEMES

In general, level shift PWM, phase shift PWM, and space vector PWM are likely the preferred control techniques for modulating MLI. The N-1 carrier signals of equal in magnitude, which run at high frequency, are compared with one reference sinusoidal signal in all level shift control techniques, including PDSPWM, PODPWM, APODPWM, VFSPWM, and PSSPWM, to produce a N level output voltage waveform. The pulse is formed when Vm > Vc for the reference axis above and when Vm < Vc for the reference axis below. Here PODPWM technique is implemented to provide better THD which are depicted in Figure 4 for (a) 5-level, (b) 7-level, and (c) 9-level systems respectively.

3.1. Proposed PWM techniques

The fundamental purpose of hybrid multilevel inverter is generating the output voltage and current with less THD. In typical POD SPWM approach, depicted in Figure 5, for solitary carrier wave frequency, volt-sec output from converter is equal. The output voltage has less THD and a pure sine wave will arise if the output volt-sec range can be reduced. By increasing the carrier frequency, in conventional multicarrier, the volt-sec can be reduced, however for some levels, the THD is not improved. Therefore, a modified multi carrier PODPWM approach is suggested here to tackle the problem mentioned above.

Here proposes a novel variable amplitude carrier SPWM technique (VASPWM). In this kind of approach, the triangle wave is created symmetrical and separated into three equal portions with varied amplitudes instead of one carrier signal Figures 6 and 7 demonstrate this. These numbers show that the duration of the pulse applied to the switch is not continuous, i.e volt-sec is reduced, which lowers conduction losses, lowers harmonics, and increases converter efficiency.

In order to obtain the variables voltage to drive a variable load, here a variable reference wave is compared with proposed carrier signal to obtain the pulses to the converter of 9-levle inverter at various modulation index values, which is shown in Figure 8, means the topology of Figure 3 can be easily operate as a 3-level, 5-level,7-level and 9-level inverter without any change of circuit topology and switching sequence, by varying the modulation index value based on load requirement.

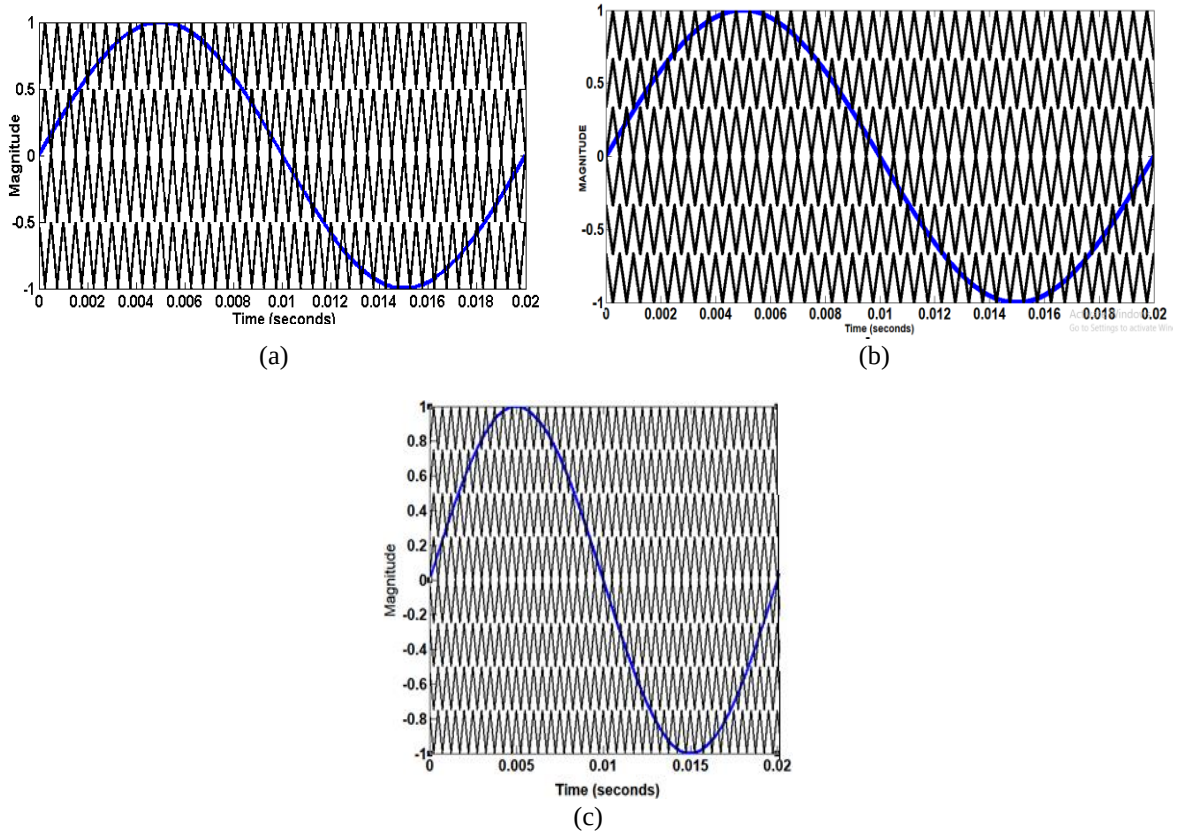

Figure 4. Conventional multicarrier PODPWM technique for (a) 5-level, (b) 7-level, and (c) 9-levels

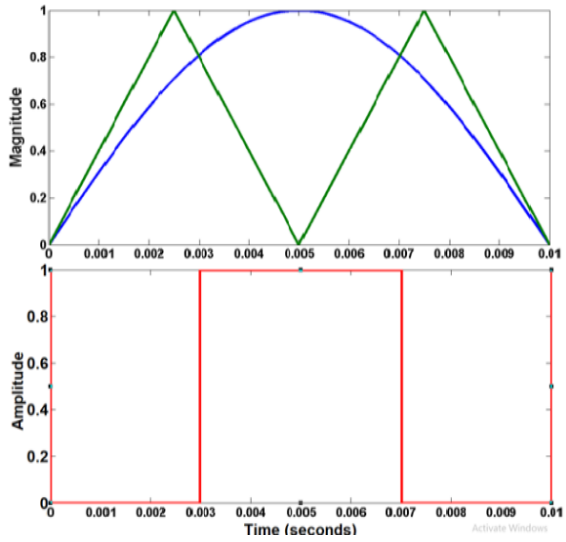

Figure 5. Pulse generation by conventional PODPWM

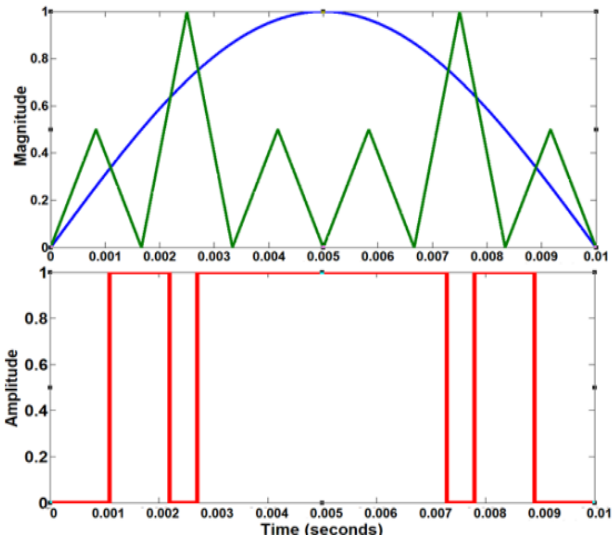

Figure 6. Pulse generation by proposed PODPWM technique

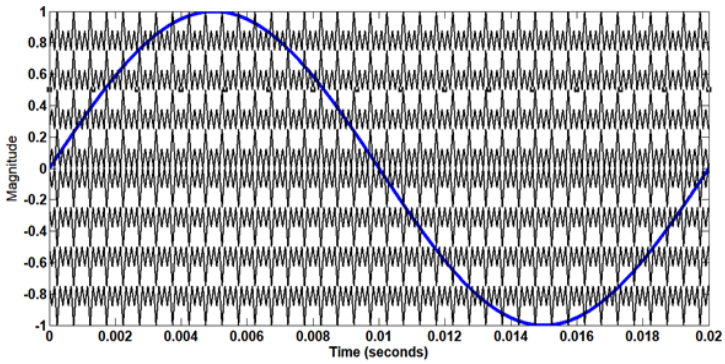

Figure 7. Variable amplitude phase opposition disposition

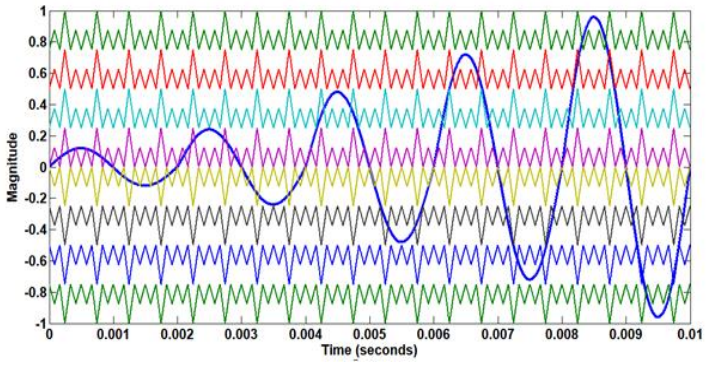

Figure 8. Variable reference wave comparison with variable amplitude multicarrier SPWM for 9-level carrier waves

4. SIMULATION RESULTS

The above-mentioned inverters' mechanism performs under normal operating circumstances are verified by MATLAB/Simulink. The variables of above inverter are listed in the Table 5. Under usual conditions, upon on the switching pattern of the converter like Table 1, the voltage transverse the R-L load and its harmonic spectrum is shown in Figure 9 and Figure 10 for conventional PODPWM technique & Figure 11 and Figure 12 for proposed PODPWM technique for 5-level operation of Figure 1. Depending on

the converter's switching configuration like Table 2, the voltage appears across R-L load and current through the load along an examination of its harmonic spectrum was shown from Figure 13 to Figure 18 for conventional and proposed PODPWM techniques for 7-level operation of Figure 2.

Table 5. Parameters of the inverter

S. No	Parameter	Value	S. No	Parameter	Value
1	Input DC voltage	200 V	4	Load resistance	50 Ω
2	Switching frequency	50 HZ	5	Load inductance	36 mH
3	Carrier frequency	2 KHZ	6	Output current	4A

According to the converter's switching configuration, as indicated in Table 3, the voltage across the R-L load and the current flowing through it together with an analysis of its harmonic spectrum were shown in Figure 19 to Figure 24 for both traditional and proposed PODPWM approaches of Figure 3 of 9-level operation. Under usual conditions, upon on the switching pattern of the converter like Table 1, the voltage transverse the R-L load and its harmonic spectrum is shown in Figure 9 and Figure 10 for conventional PODPWM technique and Figure 11 and Figure 12 for proposed PODPWM technique for 5-level operation of Figure 1. Depending on the converter's switching configuration like Table 2, the voltage appears across R-L load and current through the load along an examination of its harmonic spectrum was shown from Figure 13 to Figure 18 for conventional and proposed PODPWM techniques for 7-level operation of Figure 2. According to the converter's switching configuration, as indicated in Table 3, the voltage across the R-L load and the current flowing through it together with an analysis of its harmonic spectrum were shown in Figure 19 to Figure 24 for both traditional and proposed PODPWM approaches of Figure 3 of 9-level operation.

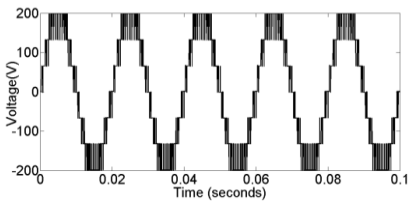

Figure 13. Output voltage of 7-level by conventional PODPWM

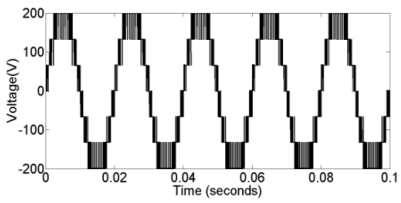

Figure 14. Output voltage of 7-level by proposed PODPWM

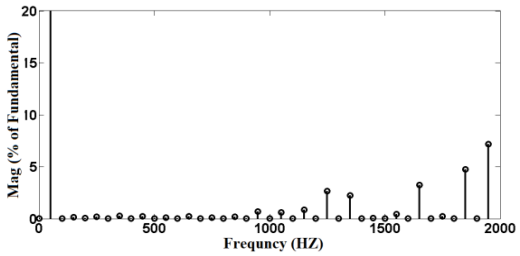

Figure 15. Harmonic spectrum of voltage of 7-level by conventional PODPWM

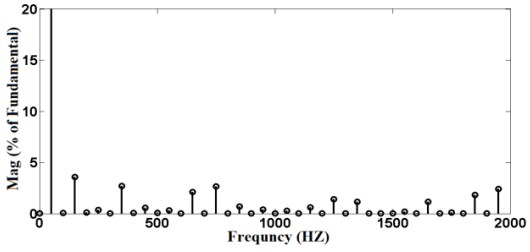

Figure 16. Harmonic spectrum of voltage of 7-level proposed PODPWM

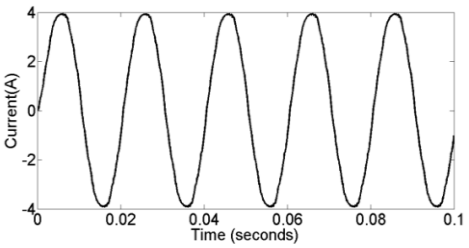

Figure 17. Output current of 7-level inverter

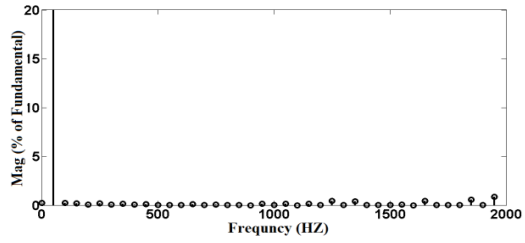

Figure 18. Harmonic spectrum of current of 7-level by proposed PODPWM

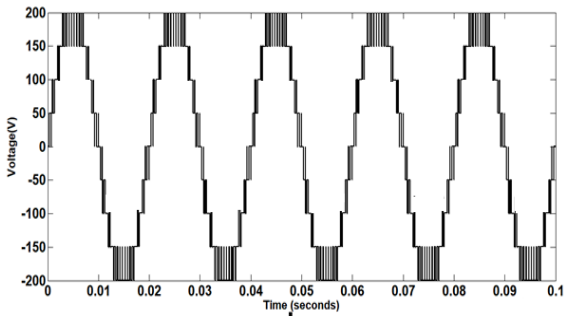

Figure 19. Output voltage of 9-level with conventional PODPWM

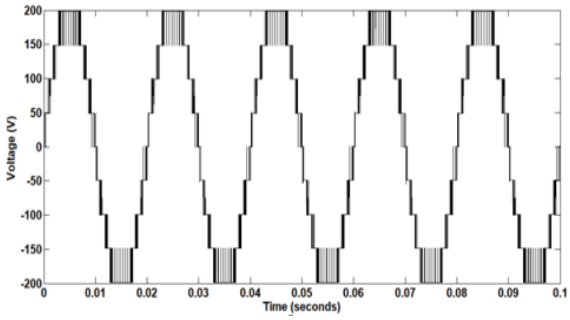

Figure 20. Output voltage of 9-level with proposed PODPWM

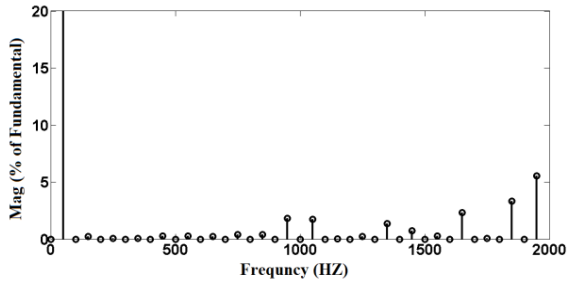

Figure 21. Harmonic spectrum of voltage of 9-level by conventional PODPWM

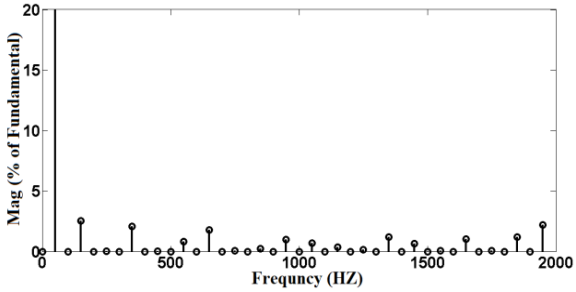

Figure 22. Harmonic spectrum of voltage by proposed PODPWM

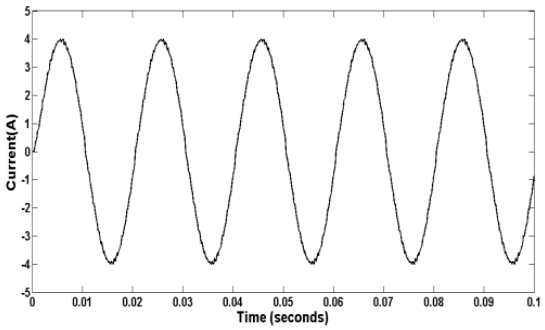

Figure 23. Output current of 9-levl with proposed PODPWM

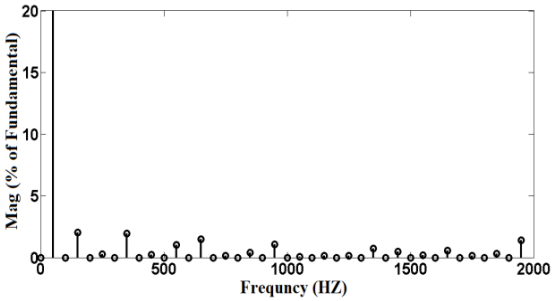

Figure 24. Harmonic spectrum of output current of 9-level by Proposed PODPWM

Figure 25 and Figure 26 shows the output voltage and current of Figure 3 at various modulation index values and observed from value of 0.1 to 0.2 it can give 3-level operation with THD 17.17%, from 0.3 to 0.5 it can be operating as a five-level inverter with THD of 9.92%, from 0.6 to 0.7 as a 7-level inverter with THD of 6.80% and from 0.8 to unity it can act a 9-level with THD of 5.04%. From this analysis it can be observed that the raise of MI value improves the both the magnitude and THD and this can be observed in Table 6 and in Figure 27. The topology of Figure 3 has a capability to operate at any voltage based on the requirement of load without change of circuit topology by the proposed PODPWM with better THD compared to other conventional PODPWM method. This THD analysis is shown in Table 7.

Table 6. Variation of voltage levels and THD at various MI values

Component	Values									
Modulation Index	0.1	0.2	0.3	0.4	0.5	0.6	0.7	0.8	0.9	1
Voltage level	3-L	3-L	5-L	5-L	5-L	7-L	7-L	9-L	9-L	9-L
Voltage Magnitude	50	50	100	100	100	150	150	200	200	200
Conventional SPWM Method (%THD)	48.01	43.08	22.95	22.54	14.73	13.5	11.86	9.64	9.18	7.51
Proposed SPWM Method (%THD)	18.31	17.17	14.63	11.13	9.92	7.45	6.80	6.43	5.87	5.04

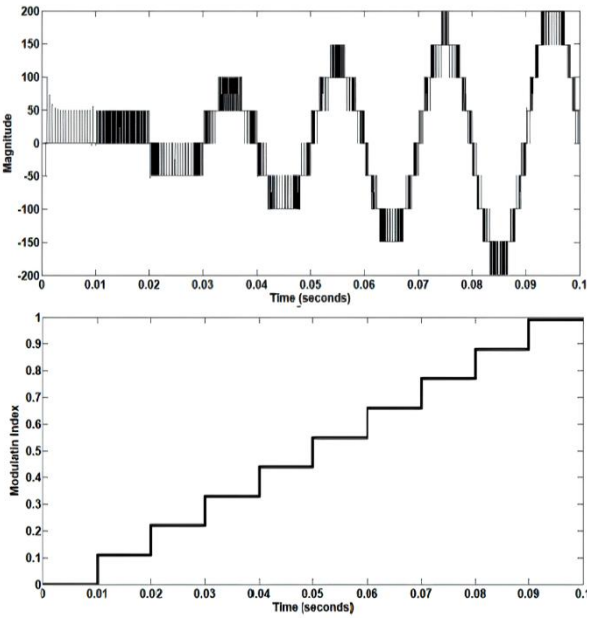

Figure 25. Output voltage of 9-level inverter at various modulation index values

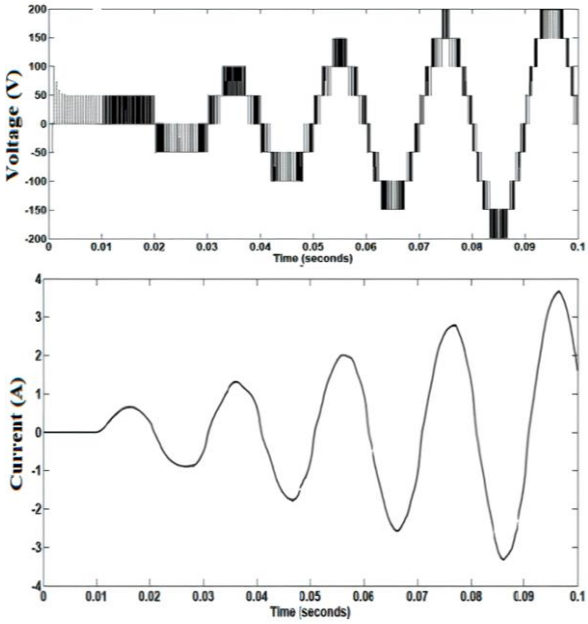

Figure 26. Output voltage and current of 9-level inverter at various modulation index

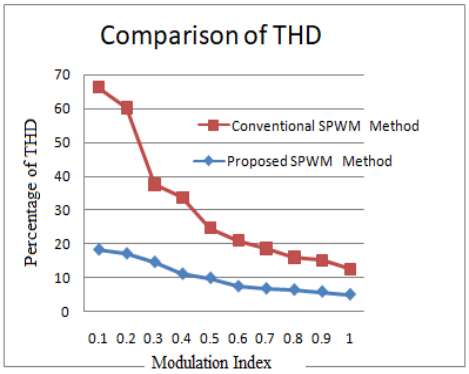

Figure 27. Comparison of THD of 9-level inverter at various modulation index values

Table 7. Comparison of THD of output voltages

PWM Technique (at Unity MI)	THD (%)		
	5-Level	7-Level	9-Level
Conventional Multi carrier POD SPWM	14.65	9.96	7.51
Proposed Multi carrier POD SPWM Technique	9.99	6.90	5.04

5. CONCLUSION

Here a novel hybrid multilevel inverter, which has capable to operate under various levels of voltages are discussed. This topology consists by 3-level diode clamped inverter and half bridge inverter with less no of devices compare to other multilevel inverters. This topology can be operating as 5-level with two equal voltage sources, as a 7-level with two unequal voltage sources and 9-level inverter with four voltage sources of equal magnitude. The modulation index decides the magnitude and THD of output voltage of the inverter, here the 9-level inverter can be operated as a variable voltage source inverter by varying the modulation index. i.e it can be operated as 3-level, 5-level, 7-level and 9-level inverter with minimum no of devices, less losses and good performance compare to other multilevel inverters. The controllability of the converter is implemented by level shifted SPWM techniques of PODPWM methods because of it gives better

performance compare to other level shifted SPWM techniques. However, the switching pulse's length is increased in the standard PODPWM approach, increasing heating losses and lowering system efficiency. In order to reduce harmonics and improve the THD of voltage and current, a modified PODPWM is suggested here. Using this method, a single carrier signal is separated into three equally sized components with unequal magnitude. The pulse's volt-sec is then decreased, increasing system efficiency by lowering the THD of the output voltage and current. So, the THD of output voltage is reduced from 7.51% to 5.04% by use of above concept of VAPODPWM technique. The 9-level inverter is valid due to act as variable inverter with fewer switches, lower costs, easier operation, and lower THD values. MATLAB/Simulink may observe this inverter's validation using a contemporary VAPODPWM.

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